WHAT IS CLAIMED IS:

1. A method of aligning an input data stream to a transmission clock in a transmitter, said method comprising:

generating a plurality of multi-phase clocks with a common frequency and multiple phases, wherein the common frequency is a sub-multiple of a data clock frequency, and the plurality of clocks is phase locked to the data clock which is synchronous with the input data stream;

demultiplexing the input data stream into a plurality of intermediate data streams using the plurality of multi-phase clocks;

generating sequence signals which are phase locked to the transmission clock, wherein the sequence signals are initialized according to a reset condition of the transmitter and the plurality of multi-phase clocks; and

multiplexing the plurality of intermediate data streams using the sequence signals, thereby constructing an output data stream which has the same data as the input data stream and is phase locked to the transmission clock.

2. The method of Claim 1, wherein the plurality of multi-phase clocks comprise of four clocks with zero degree, 90 degrees, 180 degrees and 270 degrees phase offsets; and the common speed is a quarter of the data clock speed.

3. The method of Claim 1, wherein the data clock is provided to two interconnected flip-flops to produce the plurality of multi-phase clocks.

4. The method of Claim 1, wherein the transmission clock is provided to two interconnected flip-flops to produce the sequence signals; and the flip-flops are reset by a logic circuit which receives a transmitter reset signal and at least one of the multi-phase clocks.

5. The method of Claim 1, wherein the input data stream is a multiple bits word stream; and the input data stream is aligned to the transmission clock prior to serialization of the input data stream by a clock which is phase locked with the transmission lock and has a frequency that is a multiple of the transmission clock frequency.

6. The method of Claim 1, wherein the sequence signals are initialized to avoid collisions between transitions of data in the plurality of intermediate data streams and transitions of corresponding data in the output data stream.

7. The method of Claim 1, wherein the data clock is a relatively noisy clock that is sent to the transmitter with the input data stream; and the transmission clock is a relatively quiet clock that is generated by the transmitter from a reference clock.

8. A method of demultiplexing an input data stream in a serializer, said method comprising:

receiving at a serializer, an input data stream and an input data clock;

generating multiple multi-phase clocks based on the input data clock wherein the multiple multi-phase clocks have different phase offsets; and

demultiplexing the input data stream into multiple data streams using the multiple muti-phase clocks.

9. A method of phase aligning an input data stream in a serial transmitter, said method comprising:

receiving at a serial transmitter, an input data stream and a data clock;

generating multiple multi-phase clocks based on the data clock wherein the multiple multi-phase clocks have different phase offsets;

demultiplexing the input data stream into multiple data streams using the multiple multi-phase clocks; and

multiplexing the multiple data streams based on a transmission clock, thereby constructing an output data stream which is referenced to the transmission clock.

10. The method of Claim 9, wherein the data clock and the transmission clock are independent.

11. The method of Claim 9, wherein the data clock is different from the transmission clock.

12. The method of Claim 9 further comprising initializing the multiplexing of the multiple data streams in response to a reset condition.

13. The method of Claim 9, wherein the multiplexing is sequenced to avoid collisions between transitions of data in the multiple data streams and transitions of corresponding data in the output data stream.

14. The method of Claim 9 further comprising generating sequence signals that control the multiplexing of the multiple data streams, wherein the sequence signals are based on the transmission clock.

15. A method of serializing an input data stream in a transmitter, said method comprising:

receiving at the transmitter, an input data stream and an input data clock;

generating multiple multi-phase clocks based on the input data clock wherein the multiple multi-phase clocks have different phase offsets;

demultiplexing the input data stream into multiple data streams using the multiple muti-phase clocks;

multiplexing the multiple data streams based on a transmission clock, thereby constructing an output data stream which is referenced to the transmission clock; and

serializing the output data stream.

16. A phase alignment circuit for aligning transitions in a data stream with transitions in a transmitter clock, said phase alignment circuit comprising:

a clock phase generator configured to receive a data clock which is synchronous with the data stream and to produce a plurality of demultiplex clocks which has various phase offsets;

a plurality of D-type flip-flops configured to receive the data stream in parallel and the plurality of respective demultiplex clocks to generate a plurality of respective demultiplex data streams with the various phase offsets;

a multiplexer select circuit configured to receive the transmitter clock, at least one of the plurality of demultiplex clocks, and a reset signal to produce select signals; and

a multiplexer configured to receive the select signals and to combine the plurality of demultiplexed data streams into one output datastream with transitions aligned to the transmitter clock.

17. The phase alignment circuit of Claim 16, wherein the clock phase generator further comprising:

a first flip-flop with differential data inputs, differential clock inputs, and differential outputs; and

a second flip- flop with differential data inputs, differential clock inputs, and differential outputs; wherein the outputs of the first flip-flop are coupled to the data inputs of the second flip-flop, the outputs of the second flip-flop are coupled in reversed polarity to the data inputs of the first flip-flop, and the data clock is provided to the clock inputs of the first and the second flip-flops.

18. The phase alignment circuit of Claim 16, wherein the plurality of demultiplex clocks has a frequency that is a quarter of the frequency of the data clock and has respective phase offsets of zero, 90, 180 and 270 degrees.

19. The phase alignment circuit of Claim 16, wherein the multiplexer select circuit further comprising:

a first flip-flop with differential data inputs, differential clock inputs, and differential outputs;

a second flip- flop with differential data inputs, differential clock inputs, and differential outputs; wherein the outputs of the first flip-flop are coupled to the data inputs of the second flip-flop, the outputs of the second flip-flop are coupled in reversed polarity to the data inputs of the first flip-flop, and the transmitter clock is provided to the clock inputs of the first and the second flip-flops;

a logic gate to output an initialization signal to reset the first and the second flip-flops, wherein the initialization signal is active when the reset signal is active and a select pair of the plurality of demultiplex clocks are logic high.

20. The phase alignment circuit of Claim 16, wherein the multiplexer circuit comprises a plurality of differential pair transistors.

21. A phase alignment circuit in a serial transmitter, said phase alignment circuit comprising:

a multi-phase clock generator which produces multiple clocks based on an input data clock, wherein the multiple clocks have different phase offsets;

a demultiplexer which demultiplexes an input data stream into multiple data streams using the multiple clocks; and

a multiplexer which multiplexes the multiple data streams using control signals referenced to a transmission clock.

22. The phase alignment circuit of Claim 21, wherein the data clock and the transmission clock are independent.

23. The phase alignment circuit of Claim 21 further comprising a logic circuit which initializes the control signals in response to an occurrence of a reset signal during a select phase of the multiple clocks.

24. The phase alignment circuit of Claim 21, wherein the control signals are sequenced to avoid overlapping transitions of corresponding data in the multiple data streams and the multiplexer output.

25. A phase alignment circuit comprising:

means for demultiplexing an input data stream into a plurality of intermediate data streams with a plurality of respective phases offsets, wherein the input data stream and the plurality of intermediate data streams are phase locked to an input clock;

means for generating select signals which are phase locked to a transmitter clock and initialized by a combination of a reset signal and at least one clock signal phase locked to the input clock; and

means for multiplexing the plurality of the intermediate data streams into an output data stream using the select signals, wherein the output data stream carries the same data as the input data stream and phase locks to the transmitter clock.